The Importance of Standardizing CDM ESD Test Head Parameters to Obtain Data Correlation

Leo G. Henry (1), Mark A. Kelly (2), Tom Diep (3), Jon Barth (4)

(1) ESD/TLP Consulting, P.O. Box 1665, Fremont, CA 94538, USA
Tel: 510-657-5252, Fax: 510-657-9661, e-mail: leogesd@pacbell.net

(2) Delphi Delco Electronics Systems, P.O. Box 9005, M/S R117, Kokomo, IN 46904-9005, USA
Tel: 765-451-7084, Fax: 765-451-9647, e-mail: mark.a.kelly@delphiauto.com

(3) Texas Instruments, P.O. Box 660199, M/S 8640, Dallas, TX 75266-0199, USA
Tel: 214-480-6689, Fax: 214-480-6659, e-mail: tomdiep@ti.com

(4) Barth Electronics, Inc., 1300 Wyoming Street, Boulder City, NV 89005, USA
Tel: 702-293-1576, Fax: 702-293-7024, e-mail: jonbarth@aol.com

Abstract – Parameters associated with an observed variation in CDM ESD waveforms are shown to be pogo pin diameter, pogo pin length, ground plane size, and distance between ground plane and charge plate. The effects on resulting discharge waveforms and solutions for improvement of existing CDM standards will be discussed.

Introduction

Existing CDM ESD standards [1,2] provide limited information and guidance on the parameters required to obtain repeatable, correlatable waveforms. It has been shown [3,4] that certain parameters associated with the CDM verification module (referred to as a Capacitance Only Module or COM) play a significant role in obtaining meaningful results. Some of the parameters affecting the COM design include the dielectric constant (K), disk diameter (D), and dielectric thickness (t). Investigation of the COM led to the development of a new module, the Capacitance-Inductance Module or CIM [3].

Data collected over the last several years [4,5,6] conclusively shows that an additional set of crucial parameters exists, often with undesired effects on discharge waveforms. These parameters include ground plane dimension, charge plate dimension, pogo pin diameter, pogo pin length, dielectric area, verification module disk size, and distance between the ground plane and charge plate (see Figure 1). Existing CDM standards provide limited equipment schematics; and in some cases the CDM simulator is simply defined as "must meet the waveform specified."

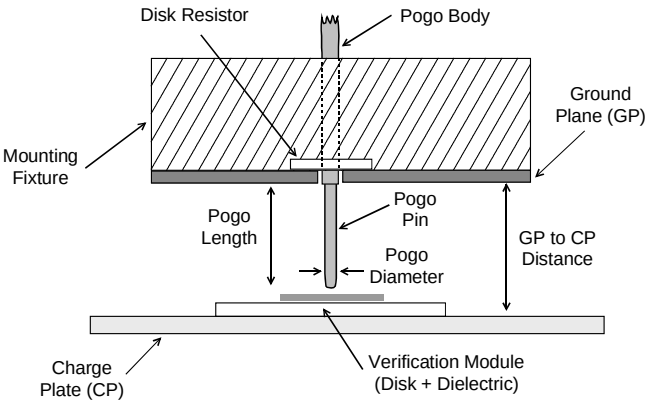


Figure 1: Illustration of crucial parameters affecting CDM event

While test standards are not designed to instruct manufacturers on how to build simulators, there is a need to provide limited guidance so that correlation can be achieved. This paper is the first attempt at providing such guidance on crucial parameters. Further examination is performed on the parameters affecting the CDM simulator. Altering these parameters is shown to dramatically change the size (e.g., peak current, etc.) and shape of the discharge waveform, possibly resulting in the simulator falling outside specification requirements. During the data collection discussed in this paper, certain conditions

(e.g., humidity, speed of approach, temperature, etc.) are assumed to be within specification requirements.

I. Experimental Set-up/Procedure

Commercial CDM test simulators from two different manufacturers were used to collect data. Discharge waveform parameters were measured using three bandwidth (BW) configurations: a stand-alone 3.5GHz BW digitizer/oscilloscope, a 1.0GHz BW digitizer/oscilloscope achieved by attaching a 1.0GHz filter to the 3.5GHz BW digitizer/oscilloscope, and a stand-alone 1.0GHz BW digitizer/oscilloscope. All digitizers/oscilloscopes were within the one year calibration period and verified prior to use.

During the verification process, a fast risetime (50ps) high voltage pulser [7] is connected to the digitizer/oscilloscope input and the response time is monitored. The results of the digitizer/oscilloscope verification were in agreement with earlier work [8]. This verification process is not intended to replace the full calibration procedure required by existing CDM standards [1,2], but merely confirms that the digitizers/oscilloscopes being used have equivalent response times.

During data collection, a minimum of 20 data points was acquired and an average value calculated. The test configuration used for waveform verification and data collection was as defined in the ESDA CDM standard [1] and illustrated in Figure 2. The influence of crucial parameters (including pogo pin diameter/length, distance between ground plane and charge plate, module disk diameter, and dielectric area) could be determined by monitoring discharge waveforms (see Figure 3).

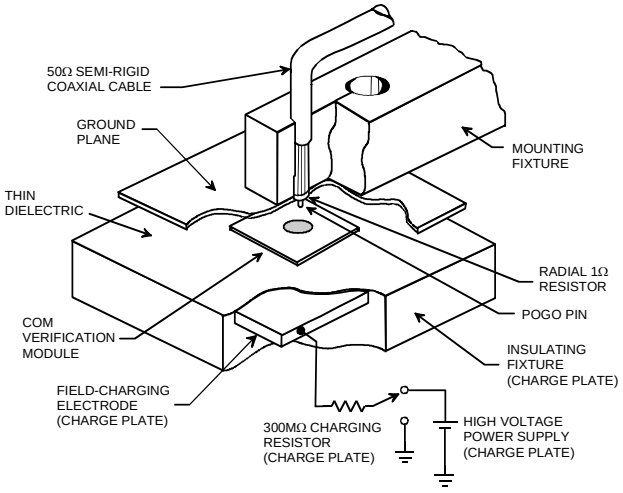


Figure 2: ESDA test configuration using COM verification module

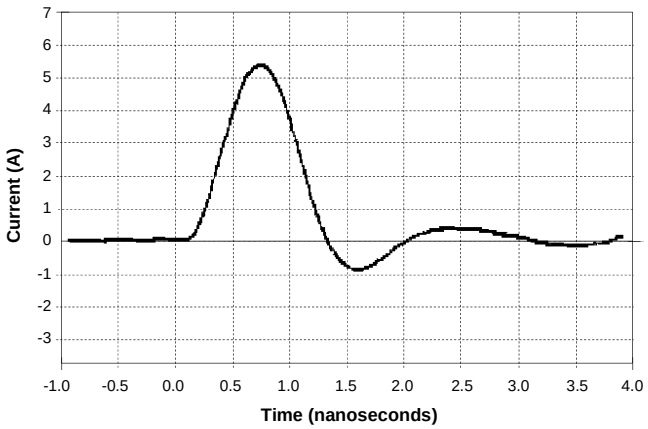
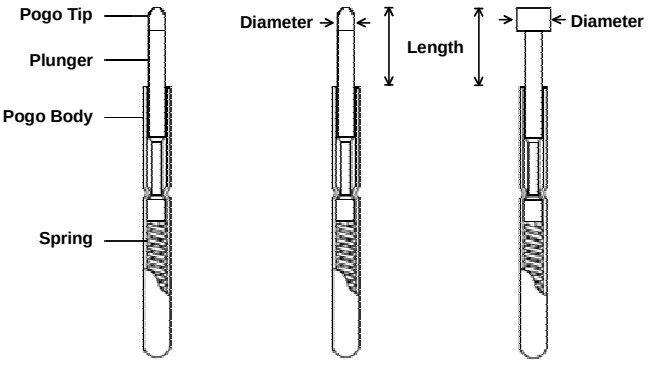


Figure 3: Typical CDM Discharge waveform

In the following sections, various objects were charged and discharged while varying certain crucial parameters. These objects included the ESDA standard COM (sections II, V, and VI), actual devices (section III), various JEDEC disks (section IV), and the Alumina CIM (section V). In this paper, we first examine the influence of spring-contact pogo pins on the discharge event. To further understand the relationship between test configuration and resulting discharge waveforms, we investigate the effects of ground plane to charge plate distance, module disk diameter, ground plane size, and module dielectric area. Finally, we review the observed results and offer solutions for improvement of existing CDM test standards.

II. Pogo Pin Effects

A significant parameter often overlooked in existing CDM standards is the spring-contact pogo pin (see Figure 4). Two key aspects of a pogo pin, pin diameter and pin length, can have a dramatic effect on the discharge event.



(a) construction (b) spherical-type (c) flat-type

Figure 4: Illustration of a spring-contact pogo pin [9]

II.a. Pogo Pin Diameter

Before CDM stressing can begin, the user must match the spring-contact pogo pin to the device lead configuration (e.g., PLCC, DIP, etc.), see Appendix Figure A1. For a PLCC-type lead configuration, a spherical pogo pin (see Figure 4b) is commonly used. The spherical-type pin allows the user to contact a specific pin under test while avoiding contact with adjacent pins. Although the spherical-type pin can be used with a variety of device pin-pitch configurations, the smallest available pogo pin diameter often exceeds the fine-pitch dimensions currently used with high pin-count devices.

For a DIP-type lead configuration, a spherical pogo pin would be difficult to use – the device lead is typically deflected by the curved tip. A better choice would be a flat pogo pin (see Figure 4c). The increased surface area associated with a flat-type pin allows the user to easily contact a specific pin under test. Unfortunately, the horizontal surface of the flat-type pin can often result in random discharge locations (e.g., center of flat surface, edge of flat surface, etc.).

Using the 4pF FR-4 verification module (COM) defined in the ESDA CDM standard [1], discharge waveforms were captured for several spring-contact pin diameters. The diameter configurations evaluated were 0.01in (0.25mm) spherical, 0.02in (0.51mm) spherical, and 0.06in (1.52mm) flat. During this investigation, the length of the pogo pin was held constant (length = 0.297in = 7.54mm), regardless of pin diameter.

A minimum of 20 data points was acquired for each pogo pin configuration using both 1.0GHz and 3.5GHz BW measurement at a charging voltage of 500V and 1000V. Table 1 shows the peak current (Ip) variation observed as different pogo pin configurations were used. The data reveals that a smaller spherical-type pin diameter produces a lower peak current (see Figure 5), regardless of voltage level or bandwidth used. For example, a 0.02in (0.51mm) pogo pin diameter produced an Ip of 5.33A while a 0.01in (0.25mm) pogo pin diameter resulted in a lower Ip value (Ip = 4.76A).

Table 1: Peak current variation as a function of pogo pin diameter (** = out of spec)

Diameter	Voltage (V)	BW (GHz)	Ip (A)
0.01in/0.25mm (spherical)	500	1.0	4.76
		3.5	7.37
	1000	1.0	9.03
		3.5	13.36
0.02in/0.51mm (spherical)	500	1.0	5.33
		3.5	7.78
	1000	1.0	9.96
		3.5	14.32
0.06in/1.52mm (flat)	500	1.0	4.97
		3.5	** 5.11 **
	1000	1.0	7.64
		3.5	** 8.01 **

As mentioned earlier, the random discharge location associated with the flat-type pogo pin can have a significant effect on the discharge event. Table 1 and Figure 5 show a lower observed peak current when the flat-type pin is used, regardless of charging voltage. Note that both spherical-type pins are within specified limits for 1GHz (3.6A to 5.4A @ 500V; 7.2A to 10.8A @ 1000V) and 3.5GHZ (6.0A to 9.0A @ 500V; 12.0A to 18.0A @ 1000V) BW measurements [1]. The flat-type pin meets the 1.0GHz BW requirement, but falls outside the acceptable limits for 3.5GHz BW measurement. Depending on the pogo pin configuration used for a given device under test, the results can vary considerably and contribute to non-correlation issues.

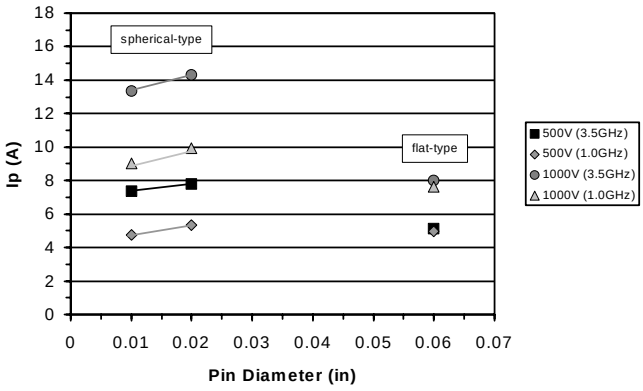


Figure 5: Peak current versus pogo pin diameter

II.b. Pogo Pin Length

Just as a user can choose from a variety of pogo tip/diameter configurations, spring-contact pogo pins are available in a variety of pin lengths. For the purposes of this investigation, the pogo pin length is

measured from the pogo body to the top of the pogo tip (as shown in Figure 4). The user can change a pogo pin's length by simply using a pin with a longer plunger (see Figure 4a). An alternate method commonly used to change a pogo pin's length is to adjust the insertion depth of the pogo body within the ground plane/mounting fixture (pogo body extends beyond the ground plane surface). Care must be taken to insert the pogo pin far enough to ensure proper contact.

Discharge waveforms were captured for various pogo pin lengths, using the same stressing procedure defined in section II.a. (4pF COM). Pogo pin lengths evaluated were 0.108in (2.74mm), 0.202in (5.13mm), 0.297in (7.54mm), 0.324in (8.23mm), and 0.488in (12.20mm). During this investigation, the pogo pin diameter was held constant (0.02in = 0.51mm spherical) regardless of pin length. A minimum of 20 data points was acquired for each pogo pin length using both 1.0GHz and 3.5GHz BW measurement at a charging voltage of 500V. Table 2 shows the peak current (Ip) variation observed as different pin lengths were used.

Table 2: Peak current variation with pogo pin length; 500V charge (** = out of spec)

BW	Length	Ip (A)	Variation
1.0GHz	0.108in (2.74mm)	** 6.85 **	35% to 53%
	0.202in (5.13mm)	** 5.76 **	
	0.297in (7.54mm)	4.95	
	0.488in (12.40mm)	4.47	
3.5GHz	0.108in (2.74mm)	** 9.57 **	35% to 53%
	0.202in (5.13mm)	** 8.95 **	
	0.297in (7.54mm)	7.63	
	0.324in (8.23mm)	6.83	
	0.488in (12.40mm)	6.25	

The data shows that a longer pogo pin produces a lower peak current, regardless of bandwidth measurement. A comparison of data resulting from the range of pogo pin lengths evaluated reveals a 35% to 53% variation for both 1.0GHz and 3.5GHz BW data (see Table 2 and Figure 6). Note that pin lengths greater than or equal to 0.297in (7.54mm) are within specified limits for 1GHz (3.6A to 5.4A @ 500V) and 3.5GHZ (6.0A to 9.0A @ 500V) measurements [1]. Although the shorter pin lengths, 0.108in (2.74mm) and 0.202in (5.13mm), fall outside the acceptable limits, the trend shown in Figure 6 remains: as pin length decreases, peak current increases (with some linearity).

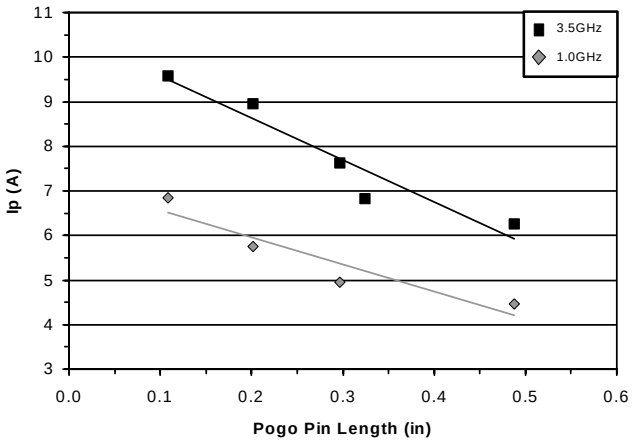


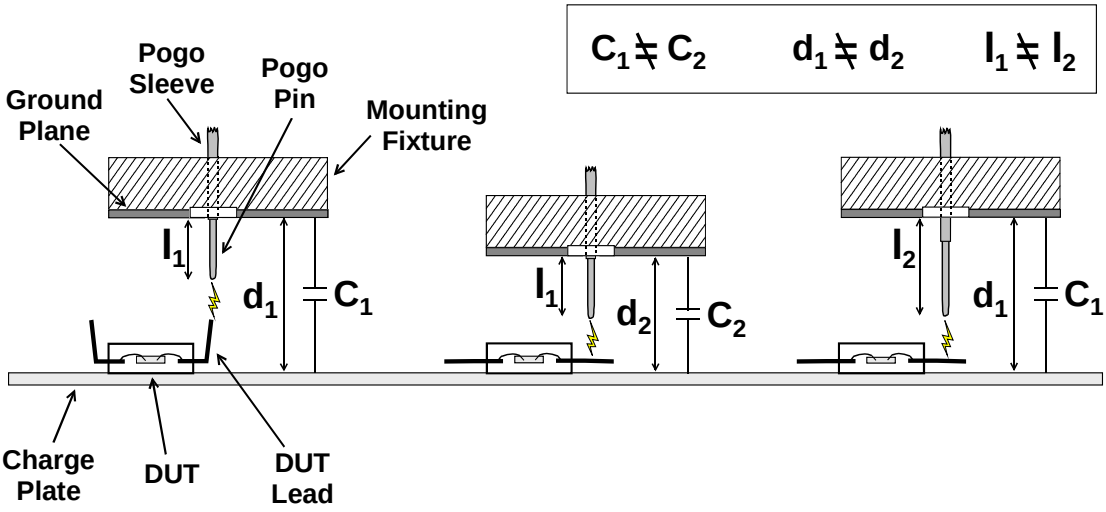
Figure 6: Peak current versus pogo pin length

These findings illustrate the importance of ensuring that pogo pin length is monitored and consistent during day-to-day usage. A pogo pin length that is too short will produce Ip values that no longer fall within specified limits. Similar to pogo pin diameter findings, test results can vary considerably depending on the pogo pin configuration used. The observed variation between the data sets, as high as 53%, can lead to significant calibration and correlation issues.

III. Distance Between Ground Plane and Charge Plate

Present CDM standards [1,2] refer to the use of a Ground Plane (GP) and Charge Plate (CP), but no specification on the distance between GP and CP exists. Device packaging in use today offers a variety of pin/lead configurations (e.g., vertical DIP, horizontal SOIC or PLCC, etc.) that determine the GP-to-CP distance. Figure 7 illustrates the relationship between GP, CP, and Device Under Test (DUT) where device leads can be vertical (replicating a DIP package) or horizontal (replicating an SOIC or PLCC package). As the device lead configuration varies (e.g., vertical to horizontal), the corresponding distance between the GP and CP changes. This distance (**d**) is a determining factor in the capacitance value (**C**) existing between the GP and CP.

Using a 500V charging voltage and 3.5GHz BW measurement, peak current (Ip) values were captured for the various configurations shown in Figure 7. To determine the effect of lead configuration, an actual device was stressed, first as a DIP (vertical leads, see Figure 7a) and then with all leads "flattened" to resemble an SOIC or PLCC (horizontal leads, see



(a) Vertical leads (b) Horizontal leads #1 (c) Horizontal leads #2

Figure 7: Illustration of pogo pin length and ground plane to charge plate distance

Figure 7b). In all lead configurations, the DUT is completely covered by the GP (2.85in x 2.50in; or 72.40mm x 63.50mm); see Figure 8.

For the purposes of this evaluation, the pogo pin diameter and length are held constant: diameter = 0.02in (0.51mm) and length = 0.105in (2.67mm). Table 3 shows the Ip variation observed when a given device's lead configuration is changed from vertical to horizontal. A vertical orientation produces an Ip of 3.38A, while the horizontal orientation results in a higher value (Ip = 4.16A).

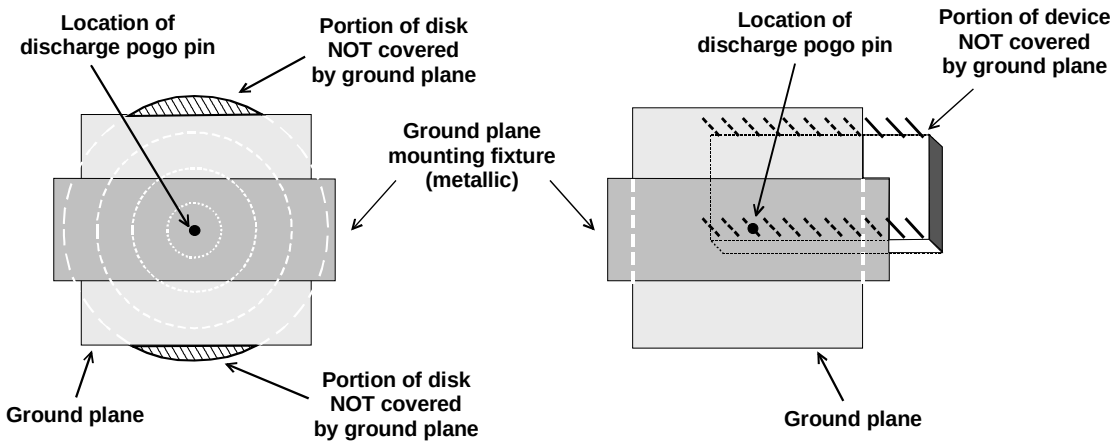
Table 3: Peak current versus distance between ground plane and charge plate (V = vertical, H = horizontal)

Object	Pogo Length	Ip	Ratio
DUT-V	0.105in (2.67mm)	3.38A	81%
DUT-H	0.105in (2.67mm)	4.16A	
4pF CIM	0.105in (2.67mm)	7.47A	83%
4pF CIM	0.205in (5.21mm)	6.23A	

With the pogo pin diameter and length constant, the crucial parameters affecting the discharge event are the distance (**d**) and corresponding capacitance (**C**) between the ground plane and charge plate. As illustrated in Figures 7a and 7b, the distance associated with the vertical orientation, $\mathbf{d_1}$, is greater than the distance for the horizontal orientation, $\mathbf{d_2}$ (or $\mathbf{d_1}>\mathbf{d_2}$). Since capacitance is inversely proportional to the distance between the plates making up a capacitor, the observed capacitance relationship of $\mathbf{C_1}<\mathbf{C_2}$ exists. Therefore, minor changes in lead configuration (that also determine the **d** and **C** values) have a dramatic effect on the discharge event. The ratio between observed Ip values (3.38A/4.16A) equals 81%, indicating that simply altering the lead orientation from vertical to horizontal (e.g., DIP to SOIC or PLCC) results in a 19% increase in Ip.

The results are similar to those observed in section II.b., where the pogo pin length was varied: a longer pin length (and thereby a greater distance between GP and CP) produced a lower peak current. To confirm those results, the above procedure was repeated using pogo pin lengths of 0.105in (2.67mm) and 0.205in (5.21mm), see Figures 7b and 7c. To minimize the effect of other crucial parameters, waveforms were obtained using a 4pF Alumina CIM [3] while holding GP size (2.85in x 2.50in; or 72.40mm x 63.50mm) and pogo pin diameter (0.02in = 0.51mm) constant (see Figure 9).

The shorter pogo pin, $\mathbf{l_1}$ = 0.105in (2.67mm), produced a peak current (Ip-short) of 7.47A, while the longer pogo pin, $\mathbf{l_2}$ = 0.205in (5.21mm), resulted in a lower peak current value (Ip-long = 6.23A). The larger Ip value corresponds to the smaller distance between GP and CP ($\mathbf{d_1}>\mathbf{d_2}$) and greater capacitance ($\mathbf{C_1}<\mathbf{C_2}$). Although the observed Ip values are within ESDA CDM standard limits (Ip = 6.0A to 9.0A @ 3.5GHz), simply increasing pogo pin length results in an Ip increase of 16% (6.23A to 7.47A). This variation will create correlation issues during round robin data collection.



(a) Coverage for various disk diameters (b) Coverage for actual device

Figure 8: Ground plane (GP) coverage illustrations

IV. Verification Module Effects

Earlier work [4] discussed the discrepancies resulting from the modules used to verify CDM discharge waveforms. The module presently used in the ESDA CDM standard [1] is the Capacitance Only Module (COM), as shown in Figure 9. This module is constructed with a gold-plated or nickel-plated, etched copper disk on single sided FR-4 dielectric material that is at least 30mm x 30mm (1.18in x 1.18in) with a thickness of 0.800mm (0.032in). A new module, the Capacitance-Inductance Module (CIM) [4], was developed to include both capacitance and inductance (see Figure 9), properties that exist in actual devices. To avoid issues associated with FR-4 (e.g., frequency dependent dielectric constant, moisture absorption, etc.), CIMs were constructed using an Alumina dielectric [4].

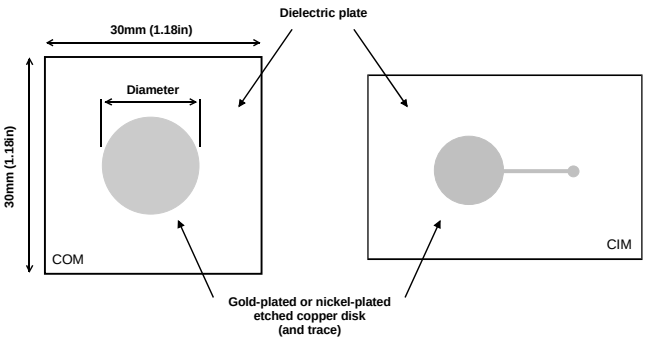


Figure 9: COM module illustration, showing disk diameter and dielectric dimensions

While COM modules have been used for some time to verify discharge waveforms, certain crucial parameters like disk diameter and dielectric area are not specified. These parameters, if left unspecified, can produce large variations in discharge waveforms; leading to repeatability and correlation problems.

IV.a. Disk Diameter

Although large and small COM verification disk diameters are specified as 26mm (1.023in) and 9mm (0.354in) respectively [1], the assumption that peak current scales linearly with disk diameter (for a given dielectric thickness) is questionable. This is especially true when other parameters are not clearly defined. To understand the effect of module disk diameter on the resulting discharge event, circular metal disks (referred to as JEDEC Disk On Plate, or DOP, modules) of various diameters were evaluated. This variation can be used to illustrate proper ground plane (GP) coverage, as shown in Figure 8a.

During this investigation, pogo pin diameter (0.02in = 0.51mm) and length (0.205in = 5.21mm) were held constant. Discharge waveforms were recorded for various disk diameters using a 500V charging voltage and both 1.0GHz and 3.5GHz BW measurement. The test configuration involved placing the DOP modules directly on the charge plate (CP), a dielectric layer of either FR-4 or Mylar material separated the metal disk from the CP. Two FR-4 dielectric thickness values were used: 20mil (0.02in = 0.51mm) and 31mil (0.031in = 0.80mm), while a 130μm (0.13mm = 0.0051in = 5.1mil) Mylar film was used. Earlier work [3] showed FR-4 material is influenced by humidity (as much as 22% moisture content) and can have a significant effect on the discharge event. Therefore, the FR-4 material was baked in a 70°C vacuum oven to remove moisture prior to use.

Results indicate that Ip increases with increasing module disk diameter, regardless of BW measurement

(see Appendix Tables A1 and A2). This trend continues until a diameter of 0.801in (20.35mm) is reached; at this value, Ip appears to "level off". By plotting peak current against (diameter)^2 values (see Appendix Figures A2 through A5), we can use the theoretical basis for capacitance [10] to visualize the increase in disk capacitance as diameter increases:

$C = E_o K A / t = E_o K (\Pi D^2) / 4t$ [Equation 1]

where, E_o = dielectric permittivity
K = dielectric constant
A = cross-sectional area
t = thickness
D = diameter

given, $I \propto C$ and, therefore, $I \propto D^2$

Figures 10 and 11 compare the results obtained for both FR-4 and Mylar using a 1.0GHz and 3.5GHz BW measurement, respectively. Although both curves follow the same trend, peak current values captured with the Mylar layer are consistently higher than those captured with the FR-4 material.

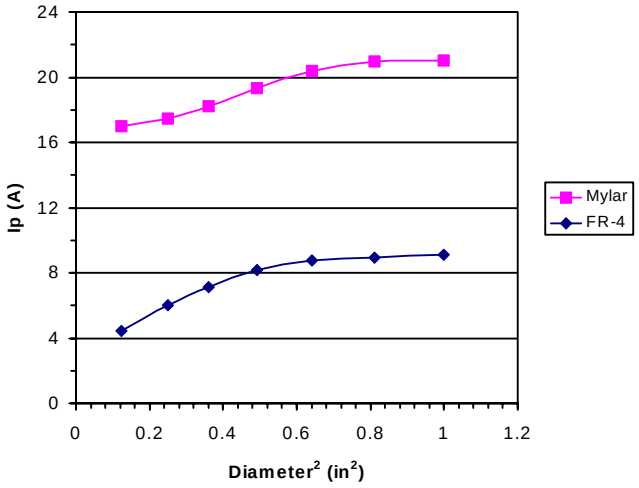


Figure 10: Peak current versus module disk (diameter)^2; FR-4 material and Mylar layer; 1.0GHz measurement

This difference illustrates the change in material parameters (e.g., thickness, K, etc.) and its effect on the discharge event. The Mylar layer thickness (130µm = 5.1mil) is much less than the FR-4 material (20mil). Therefore, the GP-to-CP distance for a Mylar layer is less than that observed with FR-4 material. As shown in section III, a shorter GP-to-CP distance will generate a higher capacitance value and, therefore, higher peak current (Ip) values.

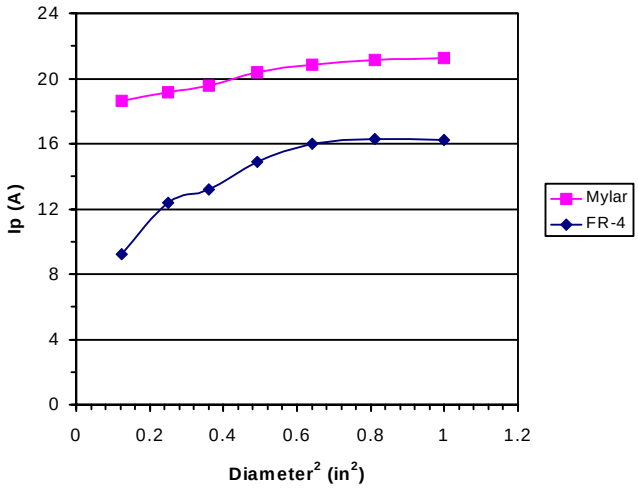


Figure 11: Peak current versus module disk (diameter)^2; FR-4 material and Mylar layer; 3.5GHz measurement

Note that the data shown in Figures 10 and 11 (see Appendix Tables A1 and A2) tends to "level off" for disk diameters > 0.801in (20.35mm). This effect may be related to insufficient ground plane coverage (see Figure 8a), where a portion of the disk is not covered by the ground plane. The result is a lower Ip value. Appendix Table A2 reveals a 1.00in (25.40mm) disk Ip value (16.25A) that is lower than the Ip value (16.30A) for a smaller disk of 0.901in (22.89mm). This finding illustrates the need for proper GP coverage (i.e., coverage beyond the edge of any device under test).

IV.b. Module Dielectric Area

The ESDA CDM standard [1] specifies a minimum COM module dielectric area, (30mm x 30mm; or 1.18in x 1.18in), but does not set an upper limit (see Figure 9). Existing manufactured modules presently used by many test facilities vary in size from (30mm x 30mm; or 1.18in x 1.18in) to (50mm x 50mm; or 1.97in x 1.97in). To investigate the effect of dielectric area, COM modules were created using three disk diameters (26mm = 1.024in; 15mm = 0.591in; and 9mm = 0.354in) and various dielectric areas. To facilitate the measurement procedure, data was collected while holding other crucial parameters constant: ground plane size (2.85in x 2.50in; or 72.40mm x 63.50mm), pogo pin diameter (0.02in = 0.51mm), and dielectric thickness (0.800mm = 0.0315in).

Peak current values were captured for each dielectric area and disk diameter configuration using 3.5GHz measurement at a charging voltage of 500V. Table 4 and Figure 12 illustrate the observed results. Note

that a slight Ip increase occurs with increasing dielectric area, regardless of disk diameter. However, the observed variation in Ip values is insignificant and should not affect lab-to-lab data correlation.

Table 4: Peak current versus increasing module dielectric area (9mm = 0.35in, 15mm = 0.59in, and 26mm = 1.02in)

Dielectric Area	Ip for a given disk diameter		
	9mm	15mm	26mm
0.188in^2 (121mm^2)	7.33A	---	---
3.26in^2 (2100mm^2)	7.53A	---	---
0.448in^2 (289mm^2)	---	12.70A	---
3.68in^2 (2376mm^2)	---	13.10A	---
1.22in^2 (784mm^2)	---	---	17.58A
3.68in^2 (2376mm^2)	---	---	18.62A

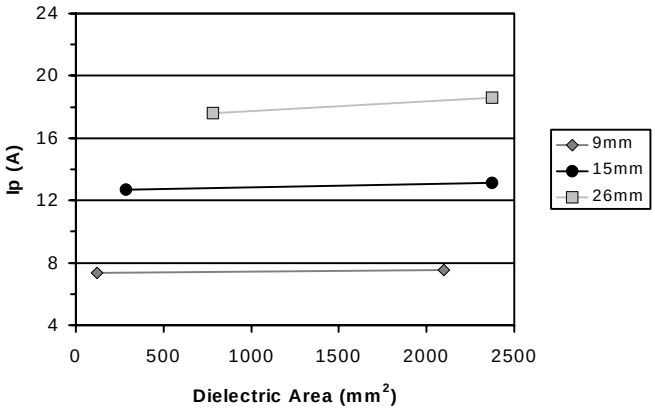


Figure 12: Peak current versus increasing module dielectric area; (9mm = 0.354in, 15mm = 0.59in, and 26mm = 1.02in)

V. Ground Plane Effects

Depending on the location of the discharge pogo pin within the ground plane (GP), a portion of the device or verification module may extend beyond the GP boundaries. This can also occur for large device packages or different module orientations (e.g., typical use versus 90° rotation of module).

Construction of most CDM simulators utilizes a mounting fixture to hold the GP in place, as shown in Figures 1, 2, and 8. The size of the mounting fixture (MF) is not specified and, in certain instances, the MF can act as an extension of the ground plane. While existing CDM standards [1,2] specify a minimum charge plate size, no specification is given for the GP; manufacturers are free to choose a ground plane configuration that is capable of producing acceptable discharge waveforms.

During the investigation performed for a previous paper [3], we observed a GP area/coverage influence on the discharge event. Waveform parameters would vary considerably depending on the GP dimension used and the verification module orientation. Rotating the module 90°, 180°, or 270° would result in significant variation. We theorized that the variation was due to GP coverage, or the percentage of the object under test that is covered by the GP.

V.a. Ground Plane Coverage

The ESDA CDM standard [1] specifies the use of two COM modules to verify discharge waveforms. In a previous paper [3], it was shown that the use of a CIM is more useful for calibration and verification purposes. However, the reported round robin data did not seem to correlate. The differences could be partly explained by inadequate GP coverage, as shown in Figures 6a and 6b.

The concept of "coverage" was investigated by capturing discharge waveforms from COM and CIM modules using different GP sizes: small (GP size = MF size) and large (GP size >> MF size). Waveforms were recorded using 3.5GHz BW measurement and a 500V charging voltage. Table 5 shows the results obtained using a 4pF and 30pF COM. Due to the symmetrical shape of the COM, the GP maintained 100% coverage regardless of GP size (small or large).

Table 5: Peak current using FR-4 COM, 100% coverage

Ground Plane (GP) or Mounting Fixture (MF)	COM Cap.	Ip (A)	Spec. Limits (A)
GP	4pF	6.99	6.0 (min) to 9.0 (max)
MF		6.73	
GP	30pF	18.10	14.4 (min) to 21.6 (max)
MF		13.24	

The findings, illustrated in Figure 13, reveal that a smaller GP will produce lower peak current (Ip) values. The effect is greater with a larger capacitance COM, where the small GP produces Ip values outside acceptable limits (6.0A to 9.0A for 4pF; and 14.4A to 21.6A for 30pF). With the lower capacitance COM, the effect is not as great; both GP sizes produce similar Ip values that are within specified limits. Although 100% coverage may exist, the data indicates a small GP can result in discharge waveforms not meeting specified limits for objects with high capacitance.

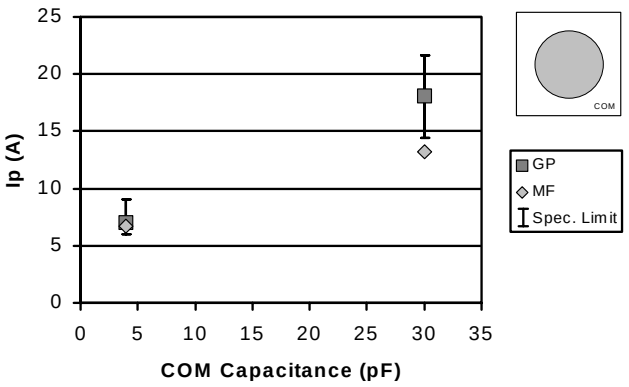


Figure 13: FR-4 COM peak current versus ground plane coverage (MF = mounting fixture, GP = ground plane)

To further understand the effect of GP coverage, the above procedure was repeated using 4pF and 35pF non-symmetrical CIMs. Again, a small (GP size = MF size) and large (GP size >> MF size) ground plane was used. Depending on the orientation of the CIM, GP coverage varied. Table 6 shows the results obtained for test configurations with 100% coverage and 60%-70% coverage. Data indicates that peak current (Ip) values decrease with inadequate coverage (<100%).

Table 6: Peak current using Alumina CIM, various coverage

Ground Plane (GP) or Mounting Fixture (MF)	CIM Cap.	GP/MF Coverage	Ip (A)
GP	4pF	100%	10.67
		60% to 70%	8.56
	35pF	100%	13.85
		60% to 70%	13.41
MF	4pF	100%	9.06
		60% to 70%	8.44
	35pF	100%	12.61
		60% to 70%	11.39

When the results are plotted (see Figure 14), we find that a large GP with 100% coverage produces a significantly higher Ip value (~2.0A greater). Note that a 20% variation in Ip values exists depending on the GP coverage and variation is independent of CIM capacitance. With the larger capacitance CIM, however, a large GP (size >> MF size) produces higher Ip values; even when compared to 100% coverage using the small GP (size = MF size). These results illustrate the importance of equivalent test configuration (e.g., GP size, module orientation, etc.) and the potential for correlation/repeatability problems.

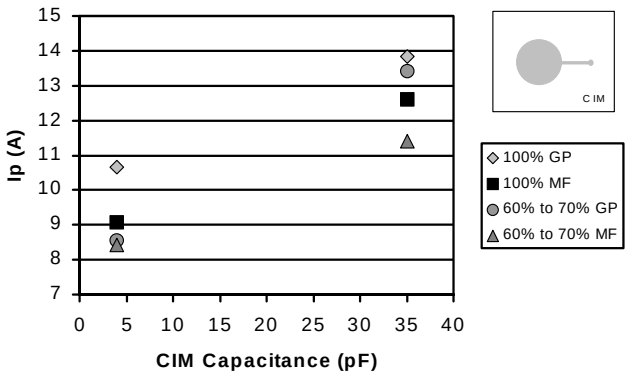


Figure 14: Alumina CIM peak current versus ground plane coverage (MF = mounting fixture, GP = ground plane)

V.b. Ground Plane Area

In section V.a., we observed variation in peak current (Ip) values resulting from ground plane (GP) size and coverage. These parameters influence the total area of the GP. As mentioned earlier, dimension specifications for the ground plane do not exist in present CDM standards [1,2]. To determine the effect of ground plane area on CDM results, data was collected using a 4pF FR-4 COM verification module and various GP configurations ranging from (0.04in x 0.04in; or 1.00mm x 1.00mm) to (0.197in x 0.197in; or 5.00mm x 5.00mm). A minimum of 20 data points were recorded for each GP configuration using both 1.0GHz and 3.5GHz BW measurement and a 500V charging voltage. Table 7 shows the Ip variation observed when a given GP area is varied.

Table 7: Peak current versus increasing ground plane area

Ground Plane Area	Ip @ 1.0GHz	Ip @ 3.5GHz
$0.0016in^2$ ($1.00mm^2$)	4.48A	7.18A
$0.0056in^2$ ($3.60mm^2$)	4.64A	7.53A
$0.011in^2$ ($7.13mm^2$)	4.98A	8.01A
$0.019in^2$ ($12.48mm^2$)	5.21A	8.11A
$0.024in^2$ ($15.21mm^2$)	5.25A	8.35A
$0.039in^2$ ($25.00mm^2$)	5.20A	8.70A

The results indicate Ip increases with increasing GP area, regardless of BW measurement. If the Ip data is plotted versus GP area, as shown in Figure 15, we can compare the results obtained using the 1.0GHz and 3.5GHz BW measurement. Note the non-linear increase in Ip with increasing GP area observed with a 1.0GHz BW measurement (identified by the flat region of the curve). This effect may be due to the bandwidth limitation of the 1.0GHz measurement

equipment [8,11]. Results for a 3.5GHz BW measurement, however, indicate an increasing Ip value as GP area increases. These findings illustrate how test data can be influenced by parameters normally thought to have little effect. Something as simple as GP size or area can have a dramatic effect on the CDM discharge event.

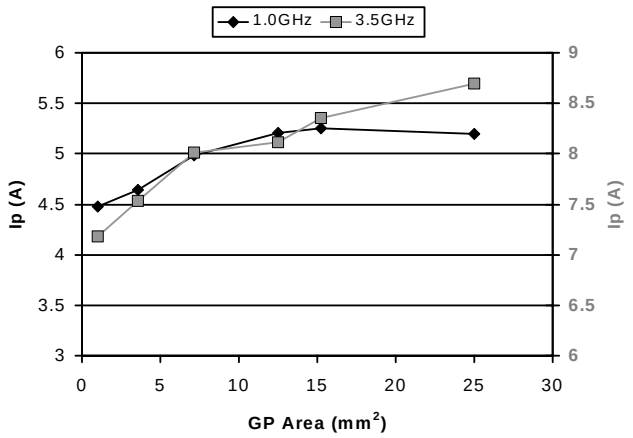


Figure 15: Peak current versus increasing ground plane area

VI. Summary

The effects of several non-electrical/physical parameters on CDM waveform peak current has been investigated. Peak current is found to increase with increasing pogo pin diameter. In contrast, pogo pin length had an opposite effect; Ip decreases with increased length. Preliminary data indicates that a long, thin pogo pin will produce a significantly reduced peak current, driving the results toward minimum acceptable limits. Conversely, a short, wide pogo pin will drive results toward maximum acceptable limits.

We've shown that the distance between the ground plane (GP) and charge plate (CP) is dependent on the combined effect of pogo pin length and type of device under test. The vertical lead configuration of a PDIP device produced a lower Ip value when compared to a flattened lead configuration of the same device due to the reduced distance between GP and CP. If a longer pogo pin is used to maintain the same distance between GP and CP, however, the lower total (overall) capacitance results in a significantly reduced Ip value.

The effect on peak current due to an increased module disk size (diameter) while maintaining adequate GP coverage is also demonstrated. Inadequate GP coverage results in a decreased peak current and deviation from the theoretical straight-line approximation. In contrast to the negligible effect of increasing dielectric area on Ip, an increase in GP area has a major effect. Data collected using 1.0GHz measurement shows an apparent "saturation" for GP area that is approximately 61% of the CP area, while data collected using 3.5GHz BW measurement continues to increase.

Acknowledgements

The authors would like to thank their support staff for collecting discharge waveform data during round-robin testing. ESDA Device Testing WG-5.0 is acknowledged for their technical support and contributions during many meetings and teleconferences. The authors would also like to acknowledge their management for their support and critical review of the paper. Special thanks are due to Bernard Hall for his input and valuable support.

References

1. "EOS/ESD-DS5.3.1-1996," ESD Association Draft Standard for Electrostatic Discharge (ESD) Sensitivity Testing – Charged Device Model (CDM) – Non-socketed Mode – Component Level, 1996.
2. "JESD22-C101," JEDEC Field-Induced Charged Device Model (FCDM) Test Method for Electrostatic Discharge (ESD) Withstand Thresholds of Microelectronic Components, May 1995.
3. L. G. Henry, M. Kelly, T. Diep, and J. Barth, "Issues Concerning CDM ESD verification Modules – The Need to Move to Alumina," EOS/ESD Symposium Proceedings EOS-21, pp. 203-211, 1999.
4. L. G. Henry and M. Kelly, Disclosure to ESDA Device Testing Committee, CDM working group WG-5.3.1, 1996 to 2000.
5. L. DeChiaro and L. G. Henry, Disclosures to ESDA Device Testing Committee, CDM working group WG-5.3.1, 1999 and 2000.
6. R. Renninger, M. Jon, D. Lin, T. Diep, and T. Welsher, "A Field-Induced Charged Device Model Simulator," EOS/ESD Symposium Proceedings EOS-11, pp. 59-71, 1989.

7. Barth Electronics, Inc., Transmission Line Pulser, model 632/732

8. L. G. Henry, H. Hyatt, J. Barth, M. Stevens, and T. Diep, "Charged Device Model (CDM) Metrology: Limitations & Problems," EOS/ESD Symposium Proceedings EOS-18, pp. 167-179, 1996.

9. Technical Application Note, "IDI Catalog and Source Book," 5th Edition, Interconnect Devices, Inc.

10. Halliday and Resnick, Fundamentals of Physics, 2nd Edition, Chapter 27, "Capacitors and Dielectrics," John Wiley Publishing, 1981.

11. Technical Application Note, "High Bandwidth Transient Capture," Tektronix Publication, 1991.

12. Halliday and Resnick, Fundamentals of Physics, 2nd Edition, Chapter 31, "Induction and Inductance," John Wiley Publishing, 1997.

13. Cletus J. Kaiser, The Inductor Handbook, 1st Edition, CJ Publishing Co., Olathe, KS, 1996.

Appendix

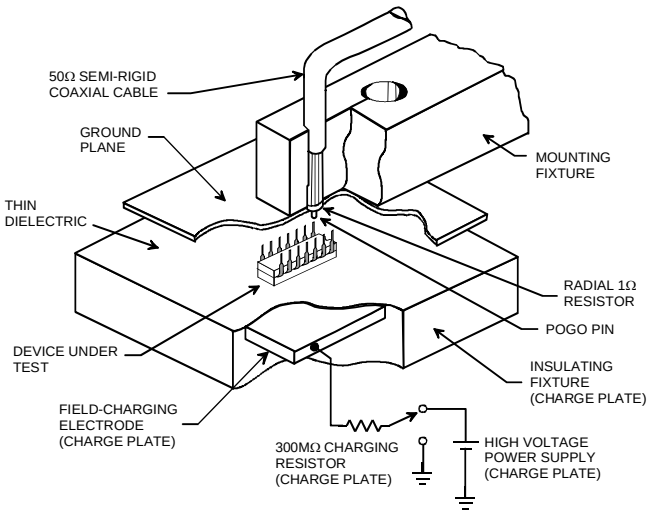


Figure A1: ESDA test configuration using actual device

Table A1: Peak current versus disk diameter; 1.0GHz measurement at 500V charge (0.02in = 0.51mm and 0.005in = 0.13mm)

Diameter	Ip – 0.02in FR-4 @ 1.0GHz	Ip – 0.005in Mylar @ 1.0GHz
0.351in (8.92mm)	4.44A	17.02A
0.501in (12.73mm)	6.01A	17.44A
0.601in (15.27mm)	7.10A	18.23A
0.702in (17.83mm)	8.15A	19.34A
0.801in (20.35mm)	8.74A	20.37A
0.901in (22.89mm)	8.96A	20.96A
1.000in (25.40mm)	9.12A	21.04A

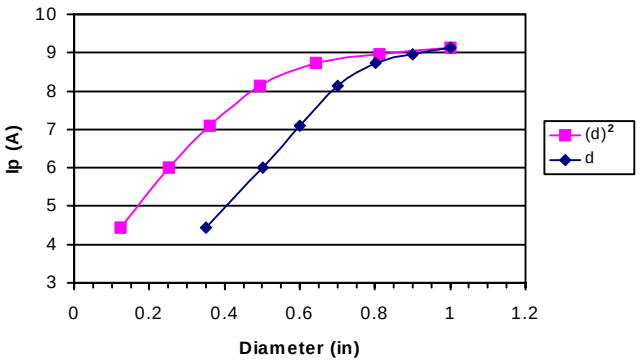


Figure A2: Peak current versus module disk diameter and (diameter)^2; FR-4 material only - no Mylar layer; 1.0GHz measurement

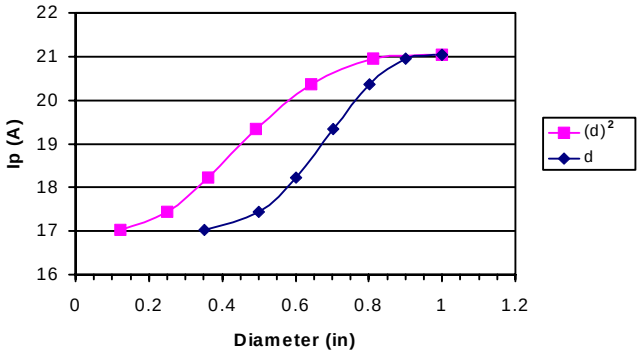


Figure A3: Peak current versus module disk diameter and (diameter)^2; Mylar layer only - no FR-4 material; 1.0GHz measurement

Table A2: Peak current versus disk diameter; 3.5GHz measurement at 500V charge (0.03in = 0.76mm and 0.005in = 0.13mm)

Diameter	Ip – 0.03in FR-4 @ 3.5GHz	Ip – 0.005in Mylar @ 3.5GHz
0.351in (8.92mm)	9.22A	18.64A
0.501in (12.73mm)	12.38A	19.17A
0.601in (15.27mm)	13.20A	19.55A
0.702in (17.83mm)	14.89A	20.37A
0.801in (20.35mm)	16.02A	20.86A
0.901in (22.89mm)	16.30A	21.16A
1.000in (25.40mm)	16.25A	21.26A

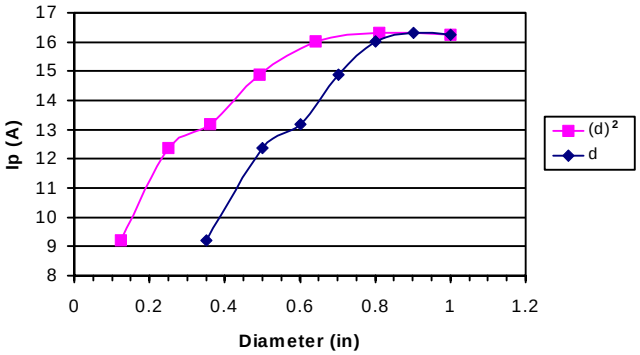


Figure A4: Peak current versus module disk diameter and (diameter)^2; FR-4 material only - no Mylar layer; 3.5GHz measurement

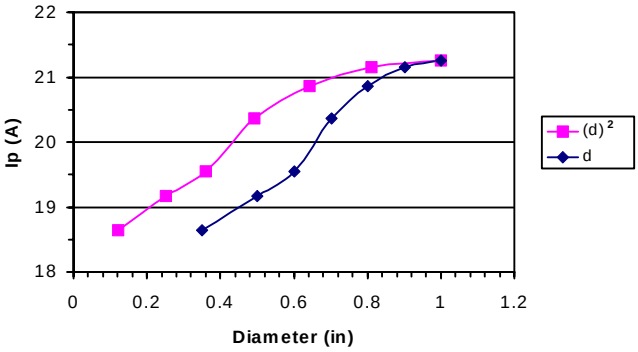


Figure A5: Peak current versus module disk diameter and (diameter)^2; Mylar layer only - no FR-4 material; 3.5GHz measurement